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VAN ROY, TOD THOMAS	

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/643,653

**Applicant(s)**

POSAMENTIER, JOSHUA D.

**Examiner**

Tod T. Van Roy

**Art Unit**

2828

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 8, 10-13 and 17-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8, 10-13 and 17-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

The examiner acknowledges the amending of claims 8, 10, and 17.

### ***Claim Objections***

The previous objection to claim 10 is withdrawn.

### ***Response to Arguments***

Applicant's arguments with respect to claims 8 and 17 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeuchi et al. (US 5563898) in view of Hirano (US 5519720).

With respect to claim 8, Ikeuchi teaches a laser to emit an optical beam (fig.10 #11), a photodiode coupled to receive the optical beam from the laser (fig.10 #21) and to convert the optical beam to a current (inherent); circuitry coupled to receive the current from the photodiode (fig.10 #16), the circuitry to adjust an amount of light output by the diode in response to a change in temperature (due to the thermistor), the circuitry including: a first resistor (fig.7 #16b, fig.7 describes the details of fig.10 #16) having a first terminal and a second terminal, the first terminal coupled to receive the current from the photodiode; a thermistor (fig.7 #16c, negative temp coeff., col.7 lines 64-66) having a first terminal connected to the first terminal of the first resistor and a second terminal directly connected to the second terminal of the first resistor (top of #16b/c); and a second resistor (fig.7 #16a) having a first terminal and a second terminal, the first terminal coupled to the second terminal of the first resistor and directly connected to the second terminal of the thermistor (bottom of #16a top of #16c), wherein current through the thermistor is to adjust in response to a change in temperature. Ikeuchi does not teach the use of an optical fiber, or to adjust for changes in the tracking. Ikeuchi also does not teach the use of a third resistor (which would be in parallel to the 1<sup>st</sup> resistor to have the desired terminal locations). Hirano teaches a semiconductor laser device which uses a fiber (which would inherently be affected differently by a temperature change when compared with the laser diode due to the differing materials), and adjusts for tracking problems (col.4 lines 43-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser emitter of Ikeuchi with the fiber of Hirano in order to facilitate the transfer of information, as well as to adjust for

Art Unit: 2828

tracking errors as is done by Hirano in order to couple the maximum amount of light possible into the fiber for optimal transmission. It would also be obvious to add a third resistor in parallel with the first resistor (accounting for the given terminal locations) as it is well known in the art that a resistance value can be split between two resistors in parallel or vice versa.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeuchi in view of Hirano and further in view of Queniat et al. (US 5383208).

With respect to claim 10, Ikeuchi and Hirano teach the apparatus as outlined in the rejection to claim 9 above, including the second circuitry having a current gain device (Ikeuchi, fig.10 #DFAI) having a first and second input, where a second input is coupled to the thermistor network (through #Q2). Ikeuchi and Hirano do not teach the first input of the gain device to be coupled to a digital to analog converter. Queniat teaches a device for controlling laser diodes wherein a digital to analog converter is used (Queniat, fig.6 #161). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the current gain device input of Ikeuchi and Hirano with the digital to analog converter of Queniat in order to allow for the input of an adjustable control signal from a digital controller (Queniat, col.4 lines 57-65) in place of Ikeuchi's fig.10 DATA value.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeuchi in view of Hirano and further in view of Queniat and Ouchi et al. (US 6055251).

With respect to claim 12, Ikeuchi, Hirano, and Queniat teach the laser apparatus as outlined in the rejection to claim 10, including the diode laser to be un-cooled (no cooling taught by Ikeuchi), but do not specify the semiconductor laser to be a distributed feedback laser. Ouchi teaches a semiconductor laser feedback system wherein a distributed feedback laser is used (col.7 lines 40-45). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser apparatus of Ikeuchi, Hirano and Queniat with the distributed feedback laser of Ouchi in order to obtain a single mode (Ouchi, col.1 lines 31-34) to allow for proper coupling to a fiber waveguide.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeuchi in view of Hirano and further in view of Queniat and Gilliland.

With respect to claim 13, Ikeuchi, Hirano and Queniat teach the laser apparatus as outlined in the rejection to claim 10, including the diode laser to be un-cooled (no cooling taught by Ikeuchi), but do not specify the semiconductor laser to be a VCSEL. Gilliland teaches a vertical cavity surface emitting laser (VCSEL) system using a feedback apparatus. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser apparatus of Ikeuchi, Hirano and Queniat with the VCSEL of Gilliland in order to allow for easier coupling to fiber optic waveguides due to the VCSEL's low beam divergence.

Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeuchi in view of Hirano and Queniat and Killian (US 6327277).

With respect to claims 17 and 20, Ikeuchi teaches the devices outlined in the rejection of claims 8 and 10 above, and the use of FETs (fig.10 #Q1/2). Ikeuchi does not teach the use of a digital to analog converter having an output coupled to the current gain device, or an integrator having an input coupled to the thermistor and resistor as well as an output coupled to the digital to analog converter. Ikeuchi also does not teach the use of an optical fiber or the use of a third resistor (which would be in parallel to the 1<sup>st</sup> resistor to have the desired terminal locations).. Hirano teaches a semiconductor laser device which uses a fiber, and adjusts for tracking problems (col.4 lines 43-67). Queniat teaches a device for controlling laser diodes wherein a digital to analog converter is used (Queniat, fig.6 #161). Killian teaches the use of an integrator in a temperature compensation system (fig.5). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser emitter of Ikeuchi with the fiber of Hirano in order to facilitate the transfer of information, as well as to adjust for tracking errors as is done by Hirano in order to couple the maximum amount of light possible into the fiber for optimal transmission (amount of light coupled will vary as the photodiode feedback increases the driving current, inherently affecting the fiber and the laser differently as the materials of the laser and fiber differ, therefor the temperature change would affect each differently), as well as to combine the current gain input of Ikeuchi with the digital to analog converter of Queniat in order to allow for the input of a control signal from a digital controller (Queniat, col.4 lines 57-65) in place of a DATA

Art Unit: 2828

reference voltage, as well as the integrator coupled to the thermistor/resistor output in order to use a cumulative feedback value rather than instantaneous (Killian, col.3 lines 54-58) avoiding unnecessarily large swings in value (thus the given circuit placement limitations would be met as the DAC output would be coupled to the current gain input through the op-amp, and the integrator output would be coupled to the DAC through the op-amp). It would also be obvious to add a third resistor in parallel with the first resistor (accounting for the given terminal locations) as it is well known in the art that a resistance value can be split between two resistors in parallel or vice versa.

With respect to claim 18, Ikeuchi further teaches the thermistor to have a negative temperature coefficient (col.7 lines 64-66).

With respect to claim 19, Ikeuchi, Queniat and Killian do not teach the integrator, DAC, and current gain device to be located on the same chip. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine these elements onto one chip in order to reduce the footprint of the overall circuit as is well known and widely practiced in the art.

### **Conclusion**

*The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.*

*US 6483625 is found to teach similar temperature compensation circuitry (fig.8), as well as US 4639924 (fig.4c) and JP 57112089 A (fig.3).*



Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2828

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR


**MINSUN OH HARVEY  
PRIMARY EXAMINER**